40V 300mA Low Quiescent Current Linear Regulator

DESCRIPTION

The VE1430Q is a high voltage, low-dropout and low quiescent current linear regulator. It operates from an input voltage of 3V to 40V.

The VE1430Q provides a wide variety of fixed output-voltage options: 3.3V, and 5.0V. Also, it provides the output-adjustable option (from 1.25V to 24V).

The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions.

The VE1430Q implements power good circuit (PG) which indicates that output voltage is in regulation. It also implements the power good delay (PGDL) circuit to program the delay time of PG signal. With these features, it can be used for power sequencing or microcontroller reset.

The VE1430Q includes thermal shutdown (TSD), current-limiting fault protection, and is available in SOIC8-EP, MSOP8-EP and SOT223 packages.

Industrial-compliant parts are available under separate datasheet (VE1430).

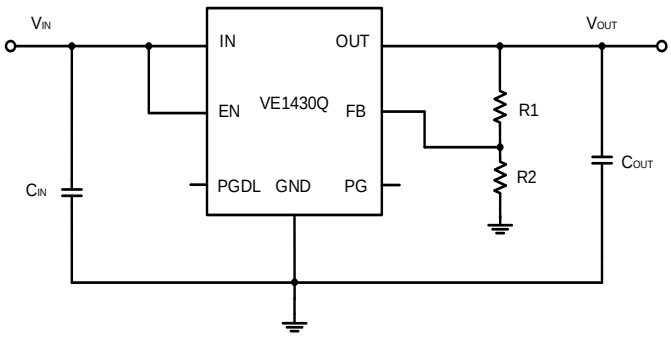
FEATURES

- AEC-Q100 qualified for automotive applications:
  – Temperature grade 1: – 40°C to 125°C, T_A
  – Junction Temperature: – 40°C to 150°C, T_J
- 3V to 40V Input Range
- 8μA Quiescent Supply Current
- Stable with Low-value Output Ceramic Capacitor (> 0.47μF)
- 300mA Specified Current
- Fixed 3.3V, 5V, and Adjustable Output (1.25V to 24V) Versions
- Output ±2% Accuracy Over Temperature
- Specified Current Limit
- Power Good
- Programmable Power Good Delay
- Thermal Shutdown and Short-Circuit Protection
- Available in SOIC8-EP,MSOP8-EP, and SOT223 packages

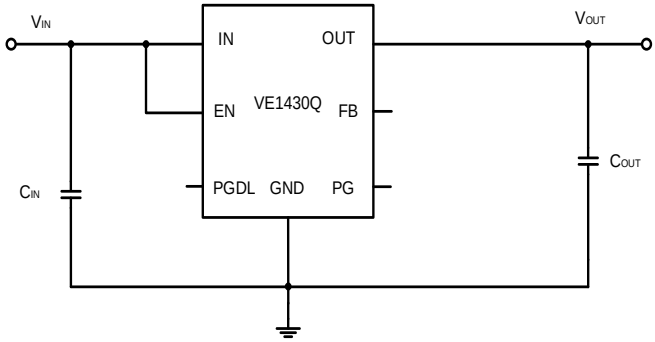
APPLICATIONS

- Automotive and Industrial Applications
- Battery-Powered Equipment
- Ultra Low-Power Microcontrollers
- Medical Imaging

TYPICAL APPLICATION

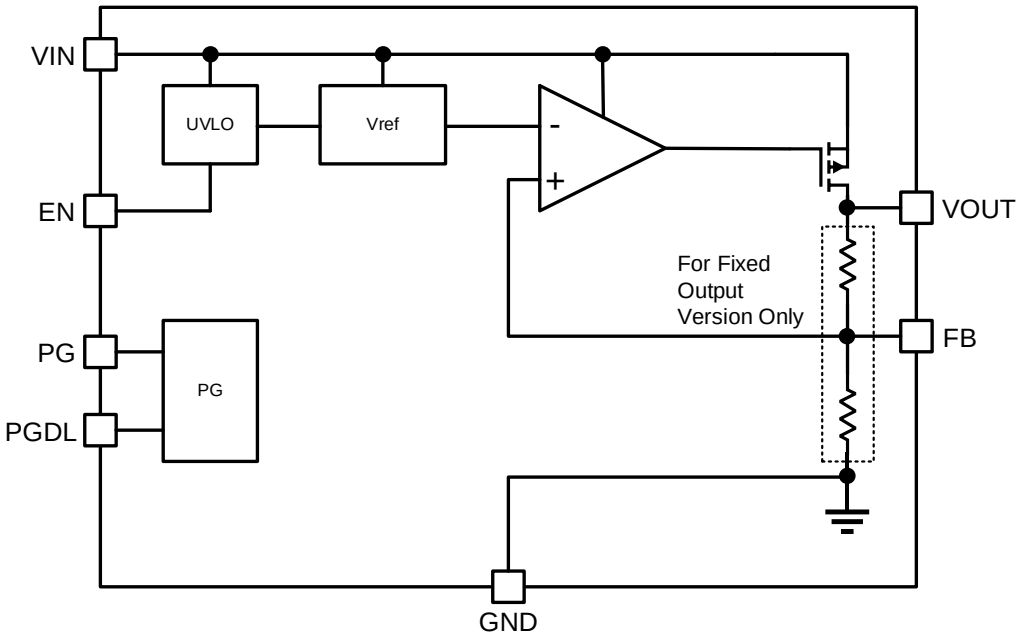


Adjustable Output



Fixed Output

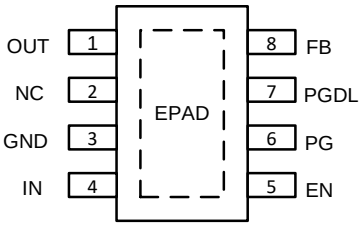
BLOCK DIAGRAM



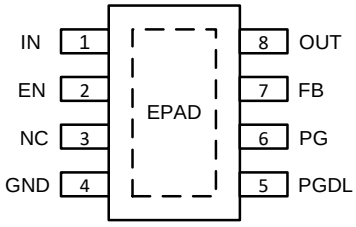
ORDERING INFORMATION

Part Number	Part Marking	Package	Packing Type	Temp Range
VE1430Q1VA1R33	1430QV33	SOIC8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1VA1R5	1430QV5	SOIC8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1VA1RADJ	1430QVADJ	SOIC8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1VA3RADJ	1430QVADJ	MSOP8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1CA3R33	1430QC33	MSOP8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1CA3R5	1430QC5	MSOP8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1BA3R5	1430QB5	MSOP8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1BA3R33	1430QB33	MSOP8-EP	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1CAFR33	1430QC33	SOT223	Tape and Reel / Detail in page 16	-40 to +125°C
VE1430Q1CAFR5	1430QC5	SOT223	Tape and Reel / Detail in page 16	-40 to +125°C

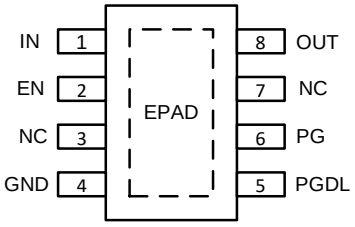
PIN CONFIGURATIONS



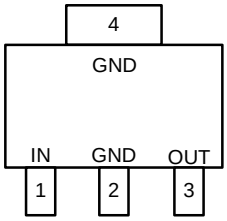
SOIC8-EP
VE1430Q1VA1



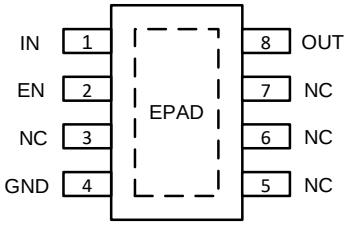
MSOP8-EP
VE1430Q1VA3



MSOP8-EP
VE1430Q1BA3



SOT223
VE1430Q1CAF



MSOP8-EP
VE1430Q1CA3

TOP VIEW

PIN DESCRIPTION

Name	SOIC8 -EP	MSOP8 -EP-V	MSOP8 -EP-B	MSOP8 -EP-C	SOT 223	Description
OUT	1	8	8	8	3	Regulated Output Voltage. Only a low-value ceramic capacitor (≥ 0.47μF) on the output is required for stability.
NC	2	3	3, 7	3, 5 6, 7	-	No Connection.
GND	3	4	4	4	2, 4	Ground. Connect the exposed pad and GND to the same ground plane.
IN	4	1	1	1	1	Input Voltage. Connect a 3V to 40V supply to V_{IN}.
EN	5	2	2	2	-	Regulator On/Off Control Input. Logic low shuts down the IC; logic high starts up the IC. Connect EN to V_{IN} for automatic start-up.
PG	6	6	6	-	-	Power Good. If not used, pin can be left floating.
PGDL	7	5	5	-	-	Programmable Power-Good Delay Time. If not used, pin can be left floating.
FB	8	7	-	-	-	Feedback Input for Output Adjustable Version. FB is regulated to 1.25V nominally. This terminal is used to set the output voltage.

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Unit
IN	-0.3	42	V
EN	-0.3	42	V
OUT	-0.3	26	V
PG	-0.3	26	V
PGDL, FB	-0.3	6	V
Junction Temperature		150	°C
Lead Temperature		260	°C
Storage Temperature	-65	150	°C

ESD RATINGS

Parameter	Value	Unit
Human Body Model (HBM), per AEC-Q100-002	3	kV
Charge Deice Model (CDM), per AEC-Q100-011	1	kV
Latch-Up, per AEC-Q100-004	100	mA

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
SOIC8-EP	50	10
MSOP8-EP	64	22
SOT223	54	10

RECOMMENDED OPERATINIG CONDITIONS

Parameter	Minimum	Maximum	Unit
Temperature	-40	125	°C
VIN to GND	3	40	V
Output	1.25	24	V

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 13.5V, T_A = -40°C to +125°C, $T_A \leq T_J \leq$ +150°C, unless otherwise noted. Typical values are at T_A=+25°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input Voltage	V_{IN}			3		40	V
Power on reset	V_{TH}				2.78		V
	V_{Hys}				0.3		V
Output Voltage Range	V_{OUT}			1.25		24	V
GND Current	I_{GND}	0 < I_{LOAD} < 1mA			8		μA
	I_{GND}	I_{LOAD} = 30mA			20		μA
	I_{GND}	I_{LOAD} = 300mA			73		μA
Shutdown Supply Current	I_S	V_{EN} = 0V		0.3	0.8	1.5	μA
Output Current	I_{OUT}			0		300	mA
Output Current Limit	I_{OC}			310			mA
Short Current Limit	I_{SC}	V_{IN} = 13.5V, V_{OUT} = 0V			220		mA
FB Voltage	V_{FB}	Adjustable output, V_{FB} = V_{OUT}, I_{LOAD} = 5mA		1.225	1.25	1.275	V
Output Voltage Accuracy		3.3V fixed output, I_{LOAD} = 5mA		3.234	3.3	3.366	V
		5V fixed output, I_{LOAD} = 5mA		4.9	5	5.1	
Dropout Voltage [1]	V_D	Adjustabe output	V_{OUT} = 5V, I_{LOAD} = 150mA, T_J = 25°C		180	300	mV
			V_{OUT} = 5V, I_{LOAD} = 300mA, T_J = 25°C		335	550	
		3.3V fixed output	V_{OUT} = 3.3V, I_{LOAD} = 150mA, T_J = 25°C		180	300	
			V_{OUT} = 3.3V, I_{LOAD} = 300mA, T_J = 25°C		335	550	
		5V fixed output	V_{OUT} = 5V, I_{LOAD} = 150mA, T_J = 25°C		180	300	
			V_{OUT} = 5V, I_{LOAD} = 300mA, T_J = 25°C		335	550	
FB Input Current	I_{FB}	Adjustable output	V_{FB} = 1.25V			50	nA
Line Regulation		Adjustable output	V_{IN} = 6V to 40V, I_{LOAD} = 5mA, V_{OUT} = 5V	-10	1	10	mV
		3.3V fixed output	V_{IN} = 5V to 40V, I_{LOAD} = 5mA, V_{OUT} = 3.3V	-10	1	10	
		5V fixed output	V_{IN} = 6V to 40V, I_{LOAD} = 5mA, V_{OUT} = 5V	-10	1	10	
Load Regulation		Adjustable output	I_{LOAD} = 5mA to 300mA, V_{OUT} = 5V,		1	15	mV
		3.3V fixed output	I_{LOAD} = 5mA to 300mA, V_{OUT} = 3.3V		1	15	
		5V fixed output	I_{LOAD} = 5mA to 300mA, V_{OUT} = 5V		1	15	
Output Voltage PSRR [2]		V_{OUT} = 5V,100Hz, C_{OUT} = 10μF, I_{LOAD} = 10mA			86		dB
		V_{OUT} = 5V,1kHz, C_{OUT} = 10μF, I_{LOAD} = 10mA			62		
		V_{OUT} = 5V,100kHz, C_{OUT} = 10μF, I_{LOAD} = 10mA			46		

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Startup Response Time		R_{LOAD} = 500Ω, V_{OUT} = 5V, C_{OUT} = 22μF, V_{OUT} from 10% to 90%		1	1.3	ms
EN Threshold Voltage	V_{IL}				0.3	V
	V_{IH}		1.3			V
EN Input Current		EN = 0V or 15V		0.1	0.5	μA
PG Rising Threshold	V_{PG_HIGH}		90%	92%	95%	V_{FB}
PG Rising Threshold Hysteresis				5%		V_{FB}
PG Low Voltage		Sink 1mA Current		0.1	0.4	V
PG Leakage Current		V_{PG} = 5V			1	μA
PGDL Charging Current	I_{PGDL}	V_{PGDL} = 1V	7.1	9.6	14.1	μA
PGDL Rising Threshold			1.4	1.8	2.5	V
PGDL Falling Threshold	V_{PGDL_LOW}		0.2	0.589	1	V
PG Delay Time	t_{PGD}	C_{PGDL} = 47nF		9.1		ms
		C_{PGDL} N/A		184		μs
PG Reaction Time	t_{PGR}	C_{PGDL} = 47nF		0.4		μs
Thermal Shutdown [2]	T_{SD}			165		°C
Thermal Shutdown Hysteresis [2]	ΔT_{SD}			20		°C

Notes:

[1] Dropout Voltage: Measured when the output voltage V_{OUT} has dropped 100mV from the nominal value.

[2] Derived from bench characterization. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1μF, C_{OUT} = 22μF, V_{IN} = 13.5V, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

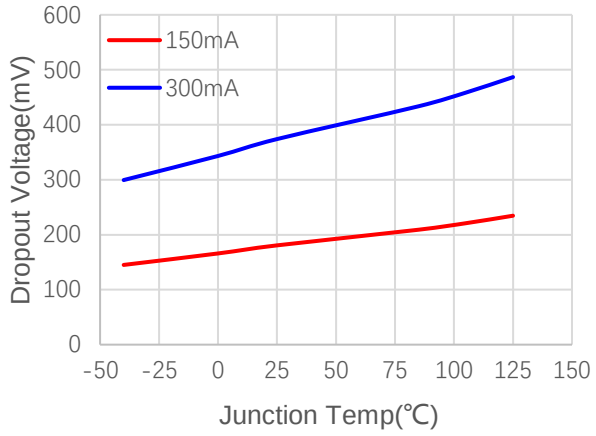


Figure 1. Dropout Voltage vs Junction Temp

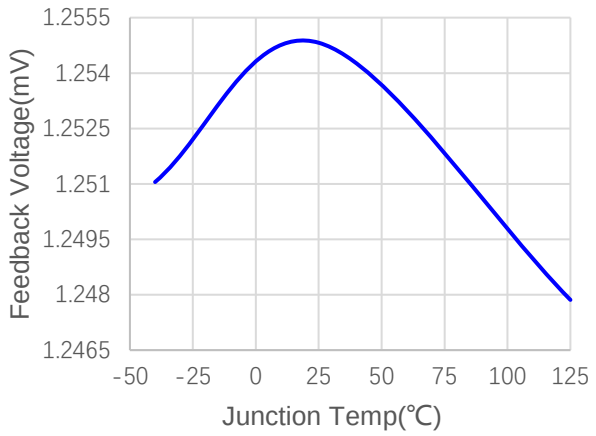


Figure 2. Feedback Voltage vs Junction Temp

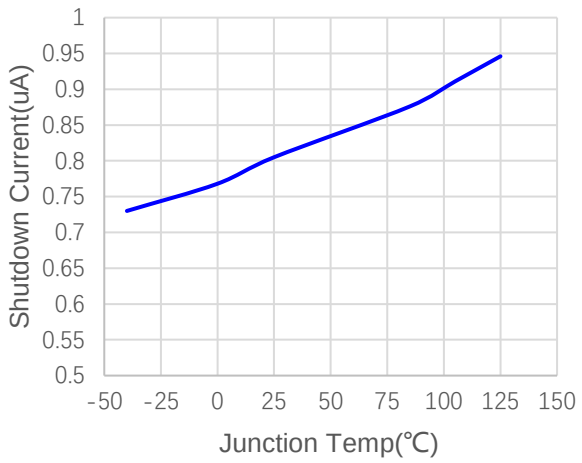


Figure 3. Shutdown Current vs Junction Temp

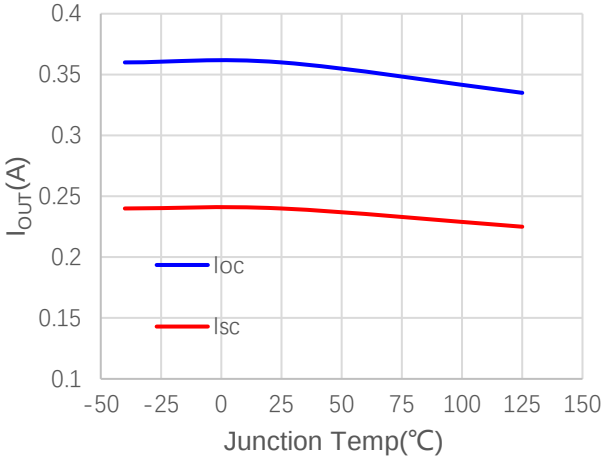


Figure 4. Current Limit vs Junction Temp

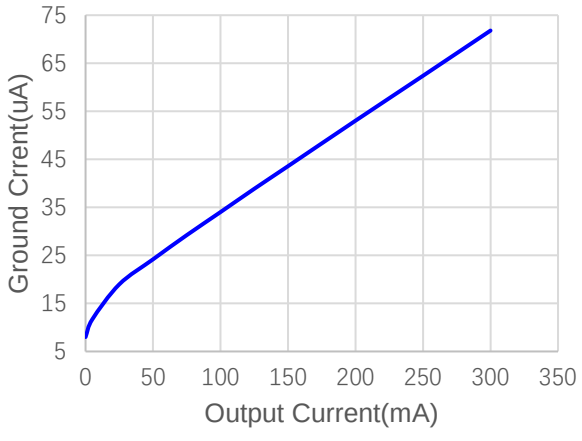


Figure 5. Ground Current vs Output Current

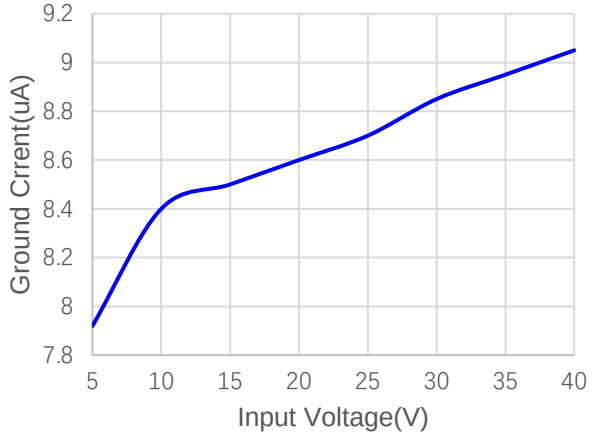


Figure 6. Ground Current vs Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1μF, C_{OUT} = 22μF, V_{IN} = 13.5V, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

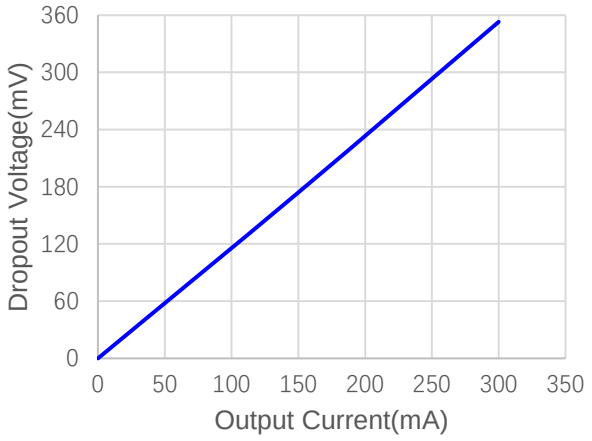


Figure 7. Dropout Voltage vs Output Current

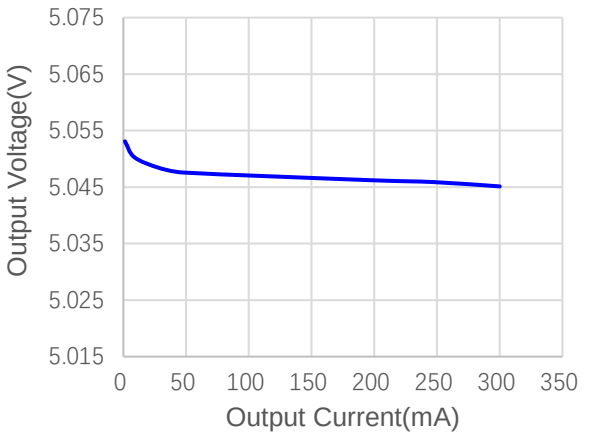


Figure 8. Output Voltage vs Output Current

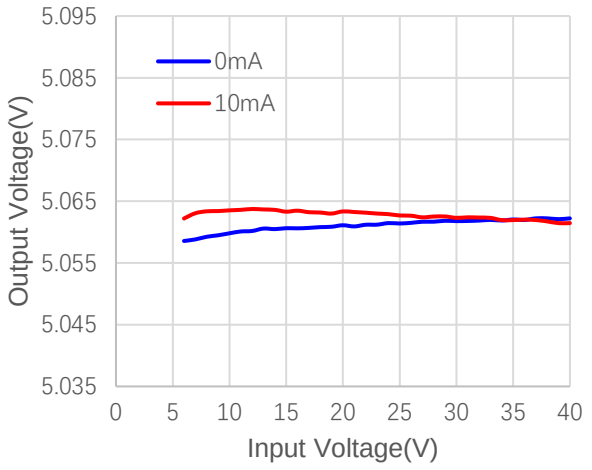


Figure 9. Output Voltage vs Input Voltage

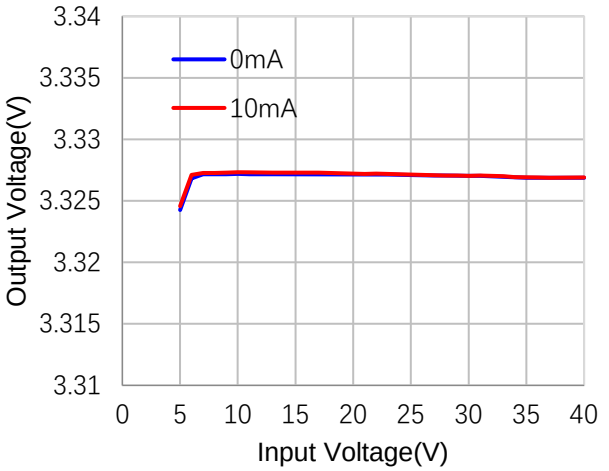


Figure 10. Output Voltage vs Input Voltage

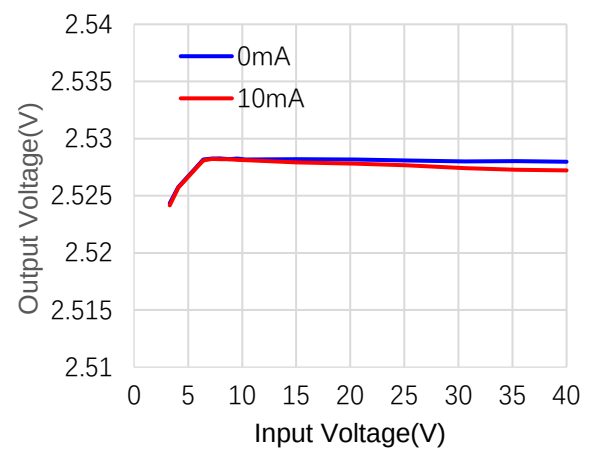


Figure 11. Output Voltage vs Input Voltage

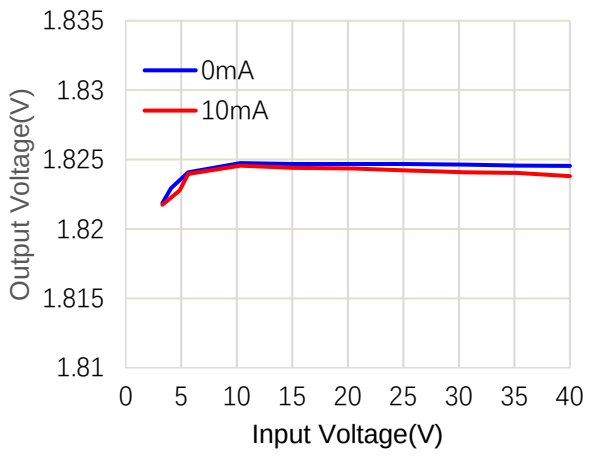


Figure 12. Output Voltage vs Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1μF, C_{OUT} = 22μF, V_{IN} = 13.5V, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

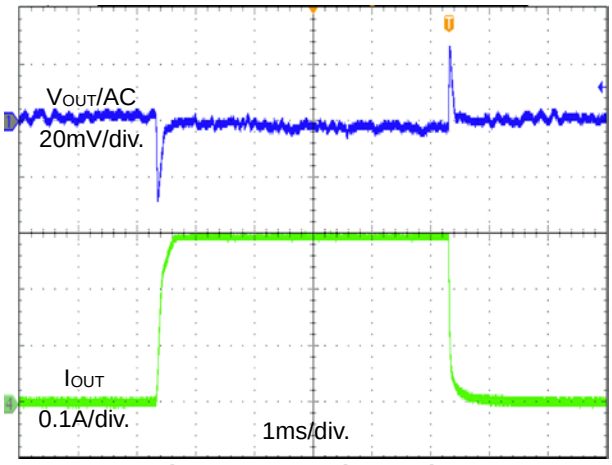


Figure 13. Load Transient
(I_{OUT} = 0~300mA)

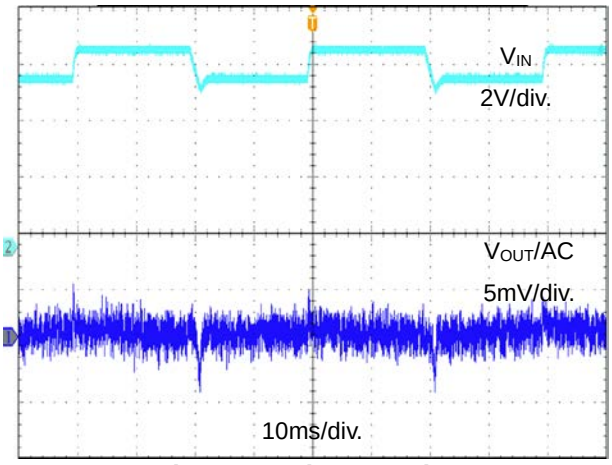


Figure 14. Line Transient
(V_{IN} = 6V-7V, I_{OUT} = 300mA)

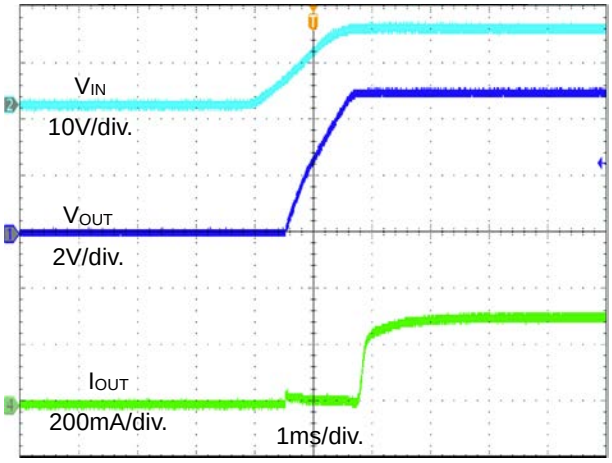


Figure 15. Start-Up Through V_{IN}
(I_{OUT} = 300mA)

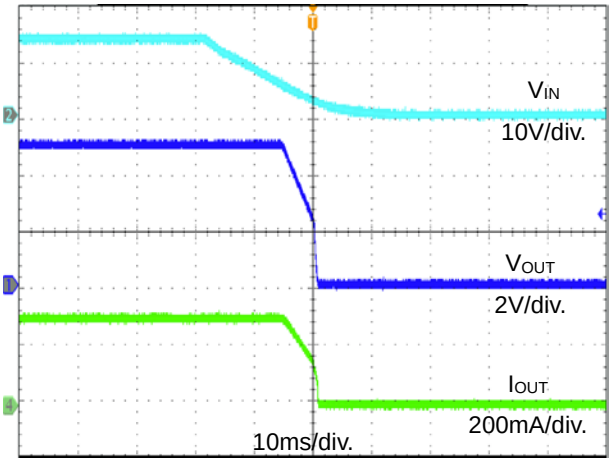


Figure 16. Shutdown Through V_{IN}
(I_{OUT} = 300mA)

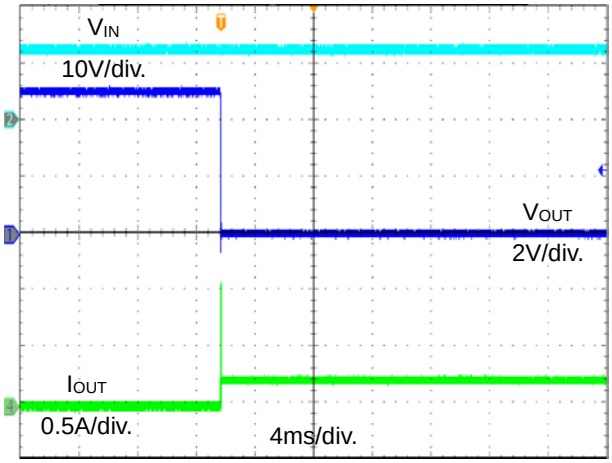


Figure 17. Short-Circuit Entry
(I_{OUT} = 0mA to short circuit)

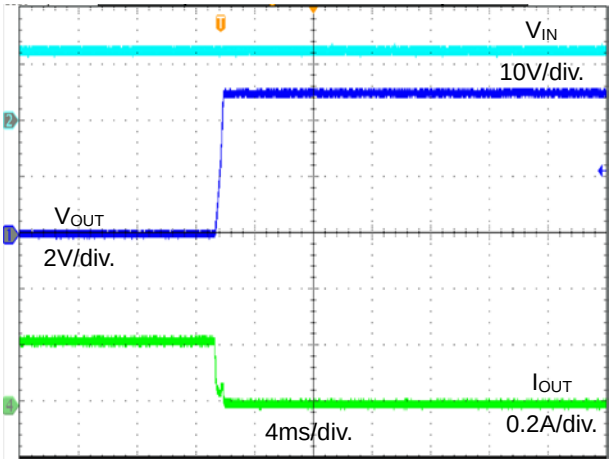


Figure 18. Short-Circuit Recovery
(short circuit to I_{OUT} = 0mA)

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1μF, C_{OUT} = 22μF, V_{IN} = 13.5V, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

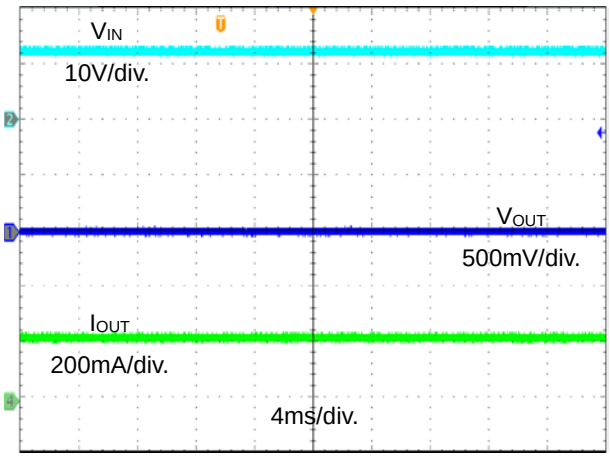


Figure 19. Short-Circuit Steady State

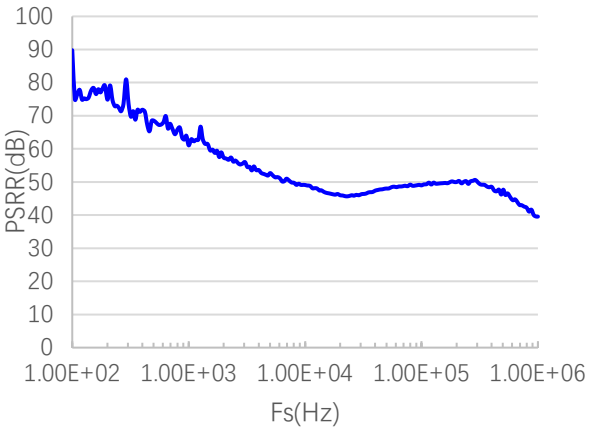


Figure 20. PSRR at 5V_{OUT} 10mA Load

FUNCTION DESCRIPTION

General Description

The VE1430Q is a linear regulator that supplies power to systems with high-voltage sources. It works in a wide 3V to 40V input range, low- dropout voltage, and a low-quiescent supply current.

The VE1430Q provides a wide variety of fixed output-voltage options: 3.3V and 5.0V. Also, it provides the output-adjustable option (from 1.25V to 24V).

The output-adjustable version has an output that is adjustable from 1.25V to 24V. It uses external feedback, allowing the user to set the output voltage with an external resistor divider. The FB threshold is 1.25V, typically.

The IC enters shutdown mode when EN is low. In shutdown mode, the pass transistor, control circuitry, reference, and all biases are turned off, which reduces the supply current to <1μA. Connect EN to V_{IN} for automatic start-up.

The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions.

The current limit is implemented by a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage $V_{FOLDBACK}$. In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit set point I_{OC}. When the output voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current limit set point. When the output is shorted, the device supplies a typical current called the short-circuit current limit I_{SC}. I_{OC} and I_{SC} are listed in the Electrical Characteristics table.

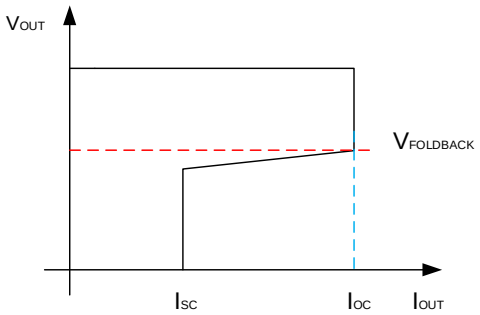


Figure 21. Current Limit with Foldback Feature

When the junction temperature is too high, the thermal sensor sends a signal to the control logic to shut down the IC. The IC will restart when the temperature has cooled down sufficiently.

The maximum output current is a function of the package's maximum power dissipation for a given temperature. The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of air flow. GND and the exposed EPAD must be connected to the ground plane for proper dissipation.

VE1430Q has one power good (PG) pin. The PG pin is the open drain of an internal MOSFET. It should be connected to V_{OUT} or external voltage source (<24V) through a resistor (i.e.100kohm). After the V_{FB} reaches 92% of nominal value, the MOSFET turns off and PG pin is pulled to high by V_{OUT} or external voltage source. When the V_{FB} drops to 87% of nominal value, the PG voltage is pulled to GND.

There is a delay time when PG asserts high. The delay time can be programmed by adding a capacitor on PGDL. To select a capacitor for PGDL, use below equation:

$$C_{PGDL}(nF) = \frac{t_{PGD}(mS) \times I_{PGDL}(\mu A)}{V_{th\_PGDL}(V)}$$

Where t_{PGD} is the desired delay time for PG asserts high, I_{PGDL} is the PGDL pin charging current and V_{th_PGDL} is 1.8V. Figure 23. shows the power good timing.

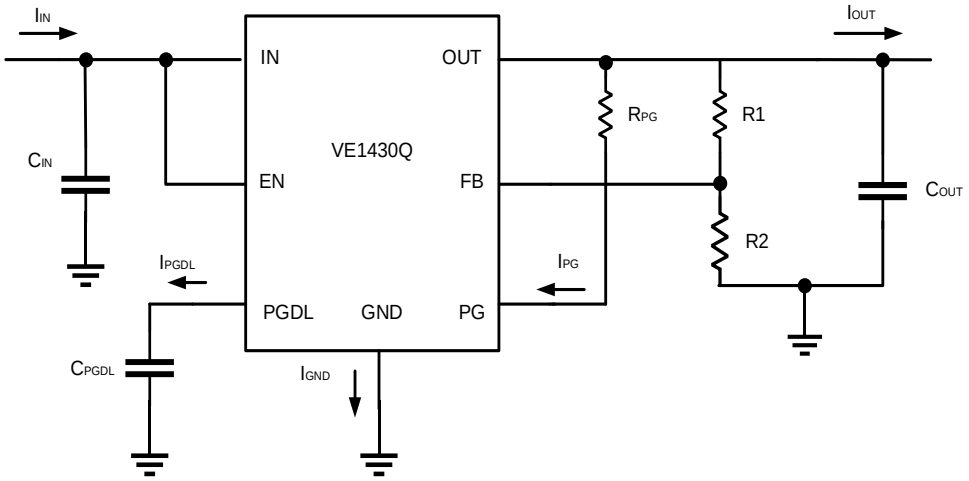


Figure 22. Application Circuit Diagram

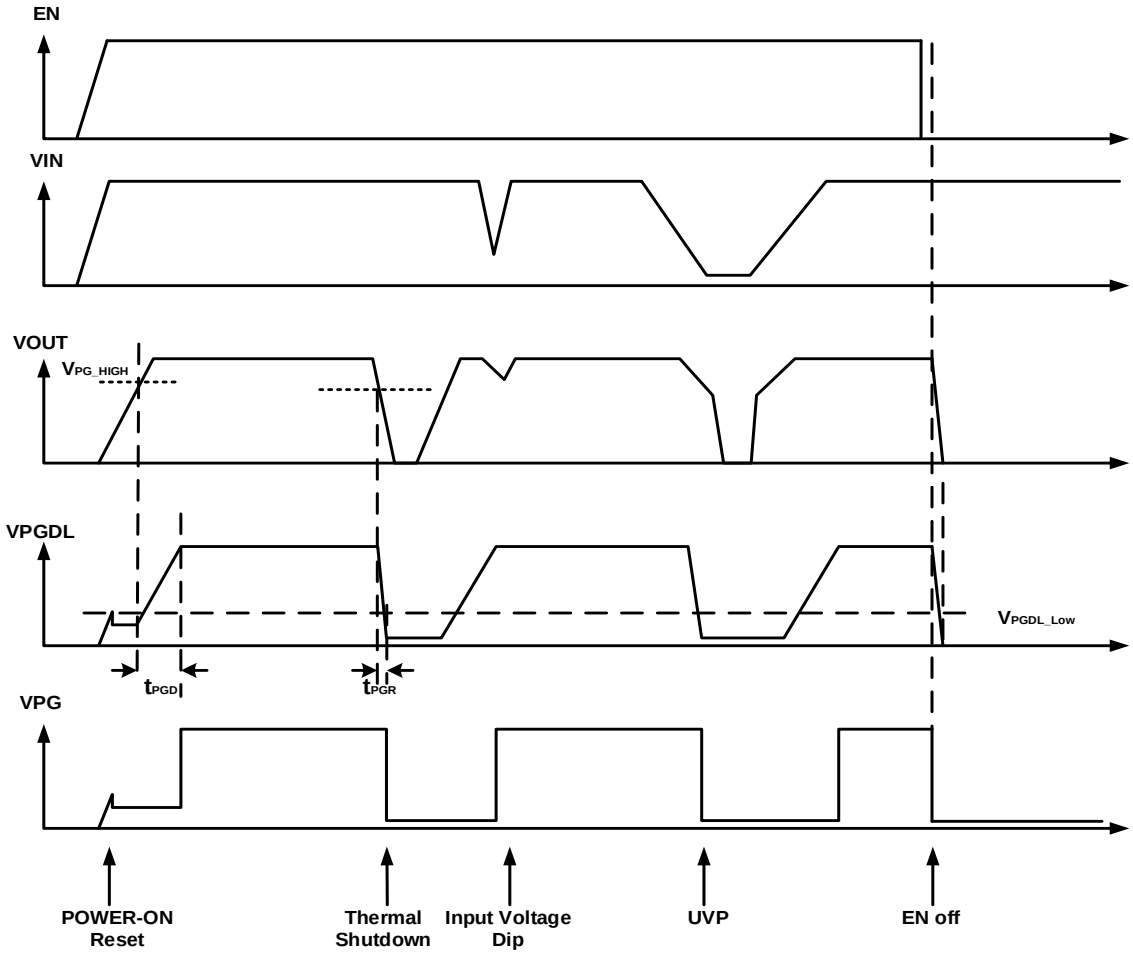


Figure 23. Power Good Timing

APPLICATION

Component Selection

Set the output voltage of the VE1430Q by using a resistor divider (see Figure24.).

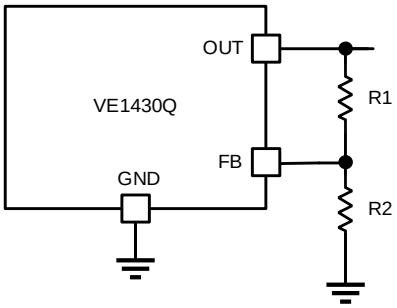


Figure 24. FB Resistor Divider to Set V_{OUT}

Choose R2 =1MΩ to maintain a 1.25μA minimum load. Calculate the value for R1 using the following equation

$$R1 = R2 \times (\frac{V_{OUT}}{1.25V} - 1)$$

For a fixed-output version, V_{OUT} can also be adjusted by adding an external resistor divider (SOIC8-EP only). When choosing an external divider, just note to take the internal FB resistor divider into consideration.

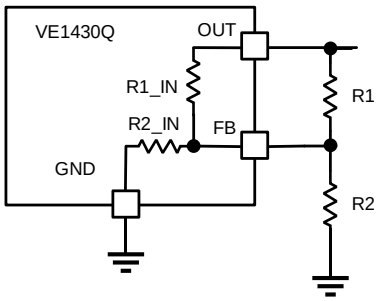


Figure25. FB Divider for Fixed-Output Version (SOIC8-EP only)

When R2 is selected, R1 can be calculated by below equation:

$$R1 = \frac{R1\_IN}{\frac{1.25 \times R1\_IN \times (R2 + R2\_IN)}{(V_{OUT} - 1.25) \times R2 \times R2\_IN} - 1}$$

The internal FB resistor dividers for different fixed- output versions are shown in below Table.

Table 1. Internal FB Resistor Divider

Fixed-Output Voltage(V)	R1_IN(MΩ)	R2_IN(MΩ)
3.3	1.476	0.9
5	2.7	0.9

Table 2 is an example of external FB divider to get various output voltages on fixed 3.3V output version.

Table 2. 3.3V External FB Divider

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)
11	80.6	10
8.5	59	10
8	54.9	10
6.5	43	10
5	30.1	10

Enable Control

EN is a digital control pin that turns the regulator on and off. When EN is pulled below 0.3V, the chip shuts down. When EN is pulled above 1.3V, the chip starts up. If this function is not used, EN can be connected to V_{IN} directly.

Input Capacitor

For efficient operation, place a ceramic capacitor (C_{IN}) between 1μF and 10μF of dielectric type (X5R or X7R) between the input pin and ground. Larger values in this range improve line transient response.

Output Capacitor

For stable operation, use a ceramic capacitor (C_{OUT}) of type X5R or X7R between 1μF and 22μF. The Larger values in this range improve load transient response and reduce noise. Output capacitors of other dielectric types may be used, but they are not recommended as their capacitance can deviate greatly from their rated value over temperature. To improve load transient response, add a small ceramic (X5R, X7R, or Y5V dielectric) feed-forward capacitor in parallel with R1. The feed-forward capacitor is not required for stable operation.

Output Noise

The VE1430Q exhibits noise on the output during normal operation. This noise is negligible for most applications. However, in applications that include analog-to-digital converters (ADCs) of more than 12 bits, consider the ADC's power supply rejection specifications. The feed-forward capacitor C_{OUT} across R1 reduces significantly the output noise.

External Reverse Voltage Protection

In some situations, e.g. a backup battery is connected as VE1430Q load, the output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is floating. Thus, the output voltage is higher than input voltage. Since the VE1430Q PMOS pass element has a body diode, a current will conduct from the output to input and is not internally limited. It's possible that the IC will be damaged by this unlimited reverse current. To avoid this, it's recommended to place an external diode at the input like below.

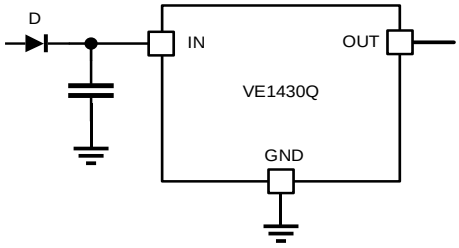
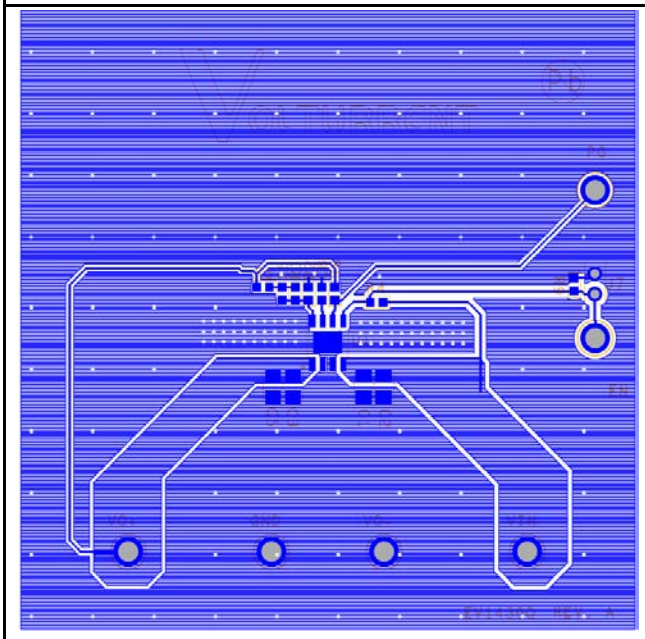
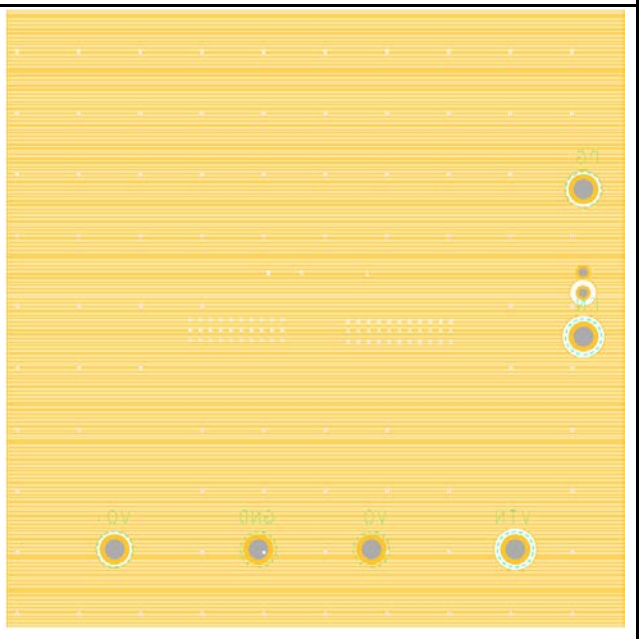


Figure 26. External Reverse Voltage protection

PCB Layout Guidelines

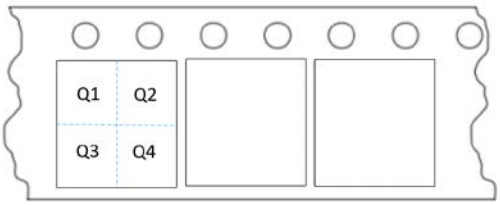
Efficient PCB layout is critical to achieve good regulation, ripple rejection, transient response, and thermal performance. It is highly recommended to duplicate the EVB layout for optimum performance. If changes are necessary, refer to below figures and follow the guidelines below: Place input and output bypass ceramic capacitors close to IN and OUT, respectively.

Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible. Connect IN, OUT, and especially, GND, respective, to a large copper area to cool the chip. This improves thermal performance and long-term reliability.

Top Layer	Bottom Layer
	

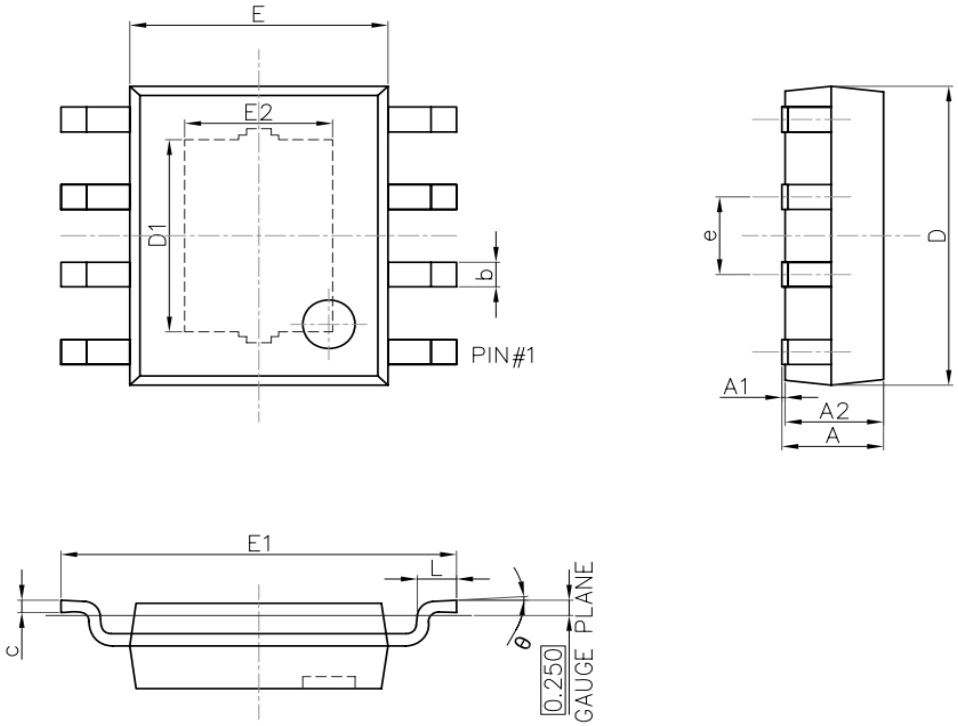
TAPE AND REEL INFORMATION

Package	Carrier Tape	Reel	Reel Color	Pin1	Qty/Reel	Reel / Inner Box	Inner Box / Outer Box	Qty/Out Box
SOIC8-EP	W=12mm, P=8mm	13inch	Blue	Q1	4000	2	8	64000
MSOP8-EP	W=12mm, P=8mm	13inch	Blue	Q1	4000	2	8	64000
SOT223	W=12mm, P=8mm	13inch	Blue	--	2500	1	8	20000



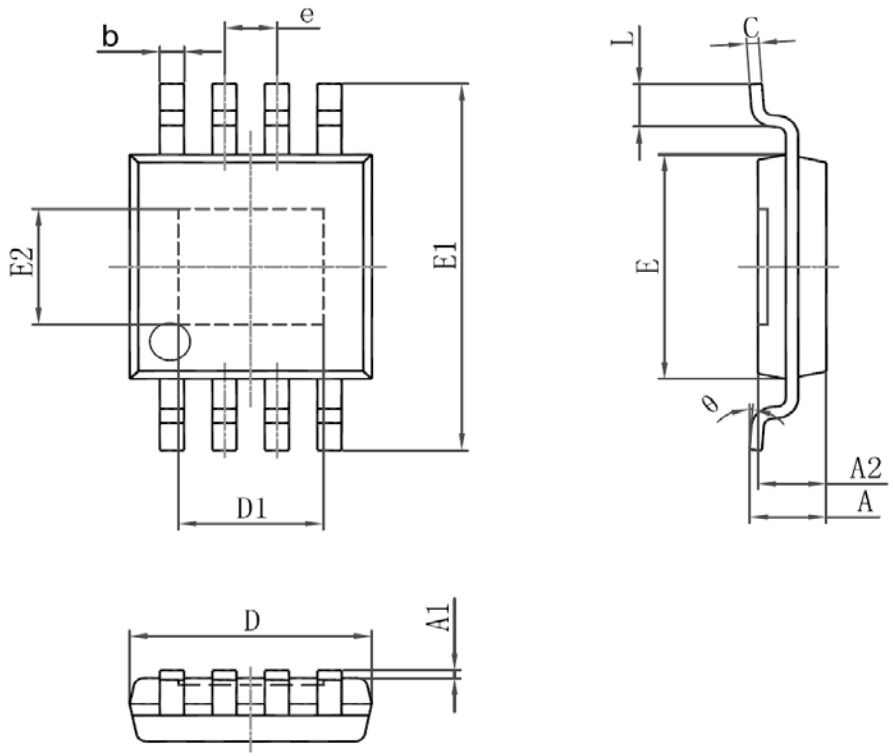
PACKAGE INFORMATION

SOIC8-EP



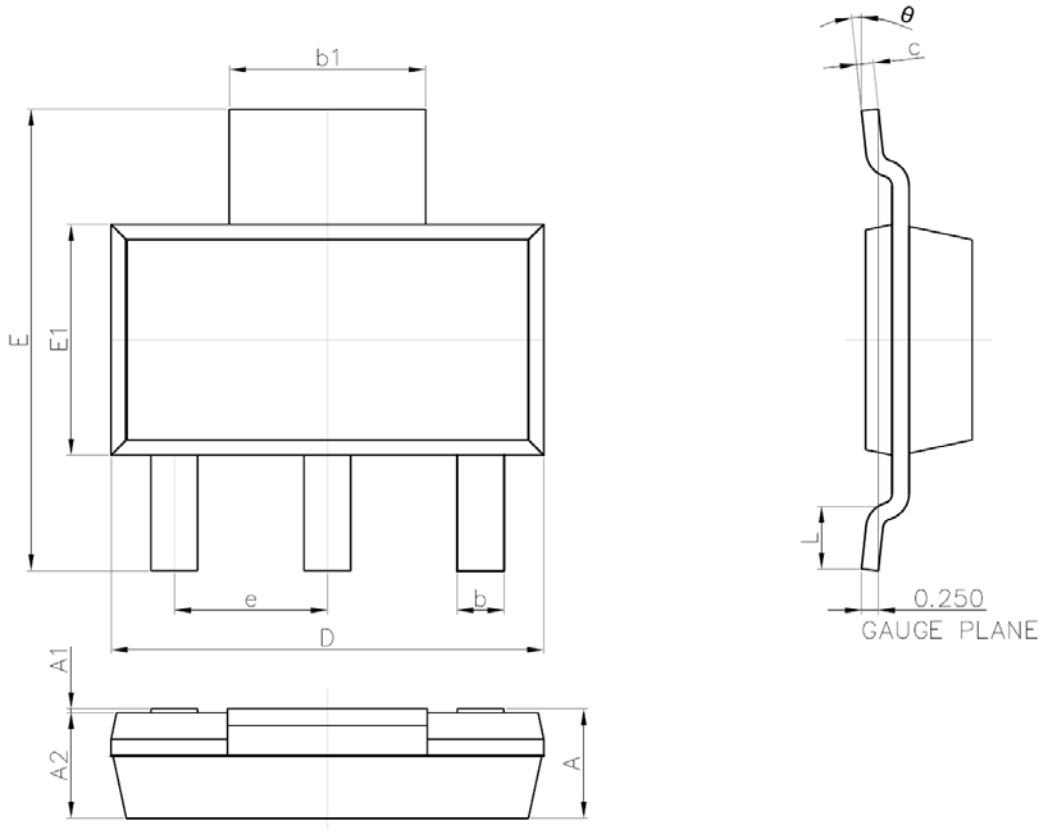
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.3	1.7	0.051	0.067
A1	0	0.1	0	0.004
A2	1.35	1.55	0.053	0.061
b	0.33	0.51	0.013	0.02
c	0.17	0.25	0.007	0.01
D	4.7	5.1	0.185	0.201
D1	3.05	3.25	0.12	0.128
E	3.8	4	0.15	0.157
E1	5.8	6.2	0.228	0.244
E2	2.16	2.36	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.4	1.27	0.016	0.05
θ	0°	8°	0°	8°

MSOP8-EP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.82	1.1	0.032	0.043
A1	0.02	0.15	0.001	0.006
A2	0.75	0.95	0.03	0.037
b	0.25	0.38	0.01	0.015
c	0.09	0.23	0.004	0.009
D	2.9	3.1	0.114	0.122
D1	1.7	1.9	0.067	0.075
e	0.65（BSC）		0.026(BSC)	
E	2.9	3.1	0.114	0.122
E1	4.75	5.05	0.187	0.199
E2	1.45	1.65	0.057	0.065
L	0.4	0.8	0.016	0.031
θ	0°	6°	0°	6°

SOT223



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.8	——	0.071
A1	0.02	0.1	0.001	0.004
A2	1.5	1.7	0.059	0.067
b	0.66	0.84	0.026	0.033
b1	2.9	3.1	0.114	0.122
c	0.23	0.35	0.009	0.014
D	6.3	6.7	0.248	0.264
E	6.7	7.3	0.264	0.287
E1	3.3	3.7	0.13	0.146
e	2.300(BSC)		0.091(BSC)	
L	0.75	——	0.03	——
θ	0°	10°	0°	10°

REVISION HISTORY

Revision	Data	Description
1.0	2024-04-18	Initial Release